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10/082,500	02/25/2002	Cheng-Lien Chiang	BDG005-3	3761

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,500	CHIANG, CHENG-LIEN	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 and 3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Upon further consideration, the election of species requirement mailed on December 17, 2002 is hereby withdrawn since the seven species identified in the restriction requirement are not patentably distinct from each other.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on February 25, 2002 and March 26, 2002 are being considered by the examiner since the submission is in compliance with the provisions of 37 CFR 1.97.

Drawings

3. The drawings are objected to because Fig. 6D is not consistent with Fig. 6B, Fig. 7D is not consistent with 7B and Figs. 10D and 10E are not consistent with Fig. 10C.

In Figs. 6B and 7B, leads are not across the top surface of a central portion 126, but the leads in Fig. 6D and 7D cross the top surface of the central portion 126.

In Fig. 10C, the metal traces 144 contact the pad 116, but the metal traces 144 in Figs. 10D and 10E do not contact the pad 116.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claims 3, 11 and 22 " the first housing portion is spaced from the upper surface," the limitation in claims 12, 17, 32, 37, 52 and 57 "the first surface contacts the light sensitive cell and the conductive trace, and the second surface ... is exposed" and the limitation in claims 16, 26, 36 and 46 "the insulative housing consisting of the first and second housing portions" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "132" in Fig. 2A has been used to designate both recessed portion and non-recessed portion, reference characters "138" and "156" in Fig. 6B have both been used to designate leads, reference characters "164" and "166" in Fig. 12C have both been used to designate top surfaces, and reference characters "184" and "186" in Fig. 13A have both been used to designate device. A proposed drawing correction or corrected

drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

7. The disclosure is objected to because of the following informalities:

On page 7, the specification needs a brief description of the drawings for Figs. 13A ~ 14B.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 12, 16, 17, 26, 32, 36, 37, 46, 52 and 57 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification

in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In claims 12, 17, 32, 37, 52 and 57, the specification fails to disclose the first surface of the second housing portion contacting the light sensitive cell and the conductive trace and the second surface of the second housing portion being exposed. Therefore, the limitation "the first surface contacts the light sensitive cell and the conductive trace and the second surface ... is exposed" must be defined in the specification or the phrase cancelled from the claims. No new matter should be entered.

In claims 16, 26, 36 and 46, the specification fails to disclose the first surface of the second housing portion contacting the light sensitive cell and the conductive trace and the second surface of the second housing portion being exposed. Therefore, the limitation "the insulative housing consisting of the first and second housing portions" must be defined in the specification or the phrase cancelled from the claims. No new matter should be entered.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1 ~ 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura et al.

Regarding claim 1, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that contacts the lower surface and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Regarding claim 2, Nakamura et al. discloses in Fig. 2 the first housing portion contacting four outer side surfaces of the chip.

Regarding claim 3, Nakamura et al. discloses in Fig. 2 the first housing portion being spaced from the upper surface.

Regarding claim 4, Nakamura et al. discloses in Fig. 2 the second housing portion contacting the conductive trace.

Regarding claim 5, Nakamura et al. discloses in Fig. 2 the second housing portion being spaced from the lower surface.

Regarding claim 6, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within the peripheral ledge.

Regarding claims 7, 15, 25 and 35, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material. Further, the limitation "wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 8, Nakamura et al. discloses in Fig. 2 the conductive trace extending through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

Regarding claim 9, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 10, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 11, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that contacts the lower surface and the side surfaces and is spaced from the upper surface and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell and is spaced from the lower surface; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Regarding claim 12, Nakamura et al. discloses in Fig. 2 the second housing portion including first and second opposing surfaces, the first surface contacts the light

sensitive cell and the conductive trace, and the second surface faces away from the chip and is exposed.

Regarding claim 13, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within the peripheral ledge.

Regarding claim 14, Nakamura et al. discloses in Fig. 2 the second housing portion being recessed relative to the peripheral ledge.

Regarding claim 16, Nakamura et al. discloses in Fig. 2 the insulative housing consisting of the first and second housing portions.

Regarding claim 17, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a cured polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed. Further, the limitation "wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se,

no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 18, Nakamura et al. discloses in Fig. 2 the conductive trace extending through a peripheral side surface of the first housing portion and contacting the second housing portion without extending through a surface of the second housing portion.

Regarding claim 19, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 20, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 21, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);

- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that provides the bottom surface and is non-transparent, and the second housing portion contacts the upper surface, provides at least a portion of the top surface and is transparent; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Regarding claim 22, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces and being spaced from the upper surface.

Regarding claim 23, Nakamura et al. discloses in Fig. 2 the second housing portion contacting the light sensitive cell and the conductive trace and being spaced from the lower surface.

Regarding claim 24, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge that forms a peripheral portion of the top surface, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 26, Nakamura et al. discloses in Fig. 2 the insulative housing consisting of the first and second housing portions.

Regarding claim 27, Nakamura et al. discloses in Fig. 2 the conductive trace and the light sensitive cell contacting a major surface of the second housing portion that faces towards and being parallel to the upper surface.

Regarding claim 28, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 29, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 30, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 31, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface, contacts the lower surface and the outer side surfaces, is spaced from the light sensitive cell and is non-transparent, and the second housing portion is a single-piece or double-piece that provides a central portion of the top surface within the peripheral portion of the top surface, contacts the first housing portion, the light sensitive cell and the conductive trace, is spaced from the lower surface and is transparent; and

- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Regarding claim 32, Nakamura et al. discloses in Fig. 2 the second housing portion including first and second opposing surfaces, the first surface faces towards the chip and contacts the light sensitive cell and the conductive trace, and the second surface faces away from the chip and provides the central portion of the top surface and is exposed.

Regarding claim 33, Nakamura et al. discloses in Fig. 2 the peripheral portion of the top surface forming a rectangular peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 34, Nakamura et al. discloses in Fig. 2 the peripheral ledge including four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

Regarding claim 36, Nakamura et al. discloses in Fig. 2 the insulative housing consisting of the first and second housing portions.

Regarding claim 37, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a cured polymeric material that is located within the peripheral ledge and includes a first surface that faces towards the chip and contacts the light sensitive cell and the conductive trace and a second surface opposite the first surface that faces away from the chip and provides the central portion of the top surface and is exposed. Further, the limitation "wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric

material" is a product-by-process claim language. Even though product- by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 38, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 39, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 40, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 41 ~ 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Kuraishi et al.

Regarding claim 41, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces,
- wherein the insulative housing further includes a first insulative housing portion (27) that covers the lower surface and is non-transparent and a second insulative housing portion (28) that covers the light sensitive cell and is transparent; and
- a conductive trace (22) that protrudes laterally from and extends through the side surface and is electrically connected to the pad.

Nakamura et al. does not disclose the conductive trace including a recessed portion that extends through the side surface and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and a corner between the side surface and the top surface. However, Kuraishi et al. discloses in Fig. 3 a conductive trace (20) including a recessed portion (18) that extends through a side surface and is spaced from a top and bottom surfaces and a non-recessed portion that extends outside an insulative housing (26) and is adjacent to the recessed portion and a corner between the side surface and the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the conductive trace as taught by Kuraishi et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a fine pattern of the inner leads (column 2, lines 8 ~ 9).

Regarding claim 42, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and four outer side surfaces of the chip.

Regarding claim 43, Nakamura et al. discloses in Fig. 2 the second housing portion contacting the light sensitive cell and the conductive trace.

Regarding claim 44, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within the peripheral ledge.

Regarding claims 45 and 55, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material, and the second single-piece housing portion being a cured polymeric material.

Further, the limitation "wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 46, Nakamura et al. discloses in Fig. 2 the insulative housing consisting of the first and second housing portions.

Regarding claim 47, Nakamura et al. discloses in Fig. 2 the conductive trace and the light sensitive cell contacting a major surface of the second housing portion that faces towards and is parallel to the upper surface.

Regarding claim 48, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 49, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 50, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 51, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces,
- wherein the insulative housing further includes a first single-piece housing portion (27) that contacts the lower surface and is spaced from the light sensitive cell and a second single-piece housing portion (28) that contacts the first housing portion and the conductive trace and is transparent, the first housing portion alone provides the bottom surface, and the first and second housing portions in combination provide the top surface; and
- a conductive trace (22) that protrudes laterally from and extends through the side surface and is electrically connected to the pad.

Nakamura et al. does not disclose the conductive trace including a recessed portion inside the insulative housing that extends through the side surface and is spaced from the top and bottom surfaces and a non-recessed portion outside the insulative

housing that is adjacent to and integral with the recessed portion and contacts the side surface and is adjacent to a corner between the side surface and the top surface. However, Kuraishi et al. discloses in Fig. 3 a conductive trace (20) including a recessed portion (18) inside an insulative housing (26) that extends through a side surface and is spaced from a top and bottom surfaces and a non-recessed portion outside the insulative housing that is adjacent to and integral with the recessed portion and contacts the side surface and is adjacent to a corner between the side surface and the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the conductive trace as taught by Kuraishi et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a fine pattern of the inner leads (column 2, lines 8 ~ 9).

Regarding claim 52, Nakamura et al. discloses in Fig. 2 the second housing portion including first and second opposing surfaces, the first surface contacts the light sensitive cell and the conductive trace, and the second surface faces away from the chip and is exposed.

Regarding claim 53, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 54, Nakamura et al. discloses in Fig. 2 the peripheral ledge including four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

Regarding claim 56, Nakamura et al. discloses in Fig. 2 the insulative housing consisting of the first and second housing portions.

Regarding claim 57, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material that includes a peripheral ledge, and the second housing portion being a polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed. Further, the limitation "wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in

"product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 58, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 59, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 60, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakaya et al. discloses in column 6, lines 11 ~ 12 a silicon film is non-transparent.

Yamanaka, Glenn, Uchiyama, Mori et al., Maekawa, Hallenbeck et al. and Arimoto disclose a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
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c.c.
April 4, 2003

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